An Environmentally Protected Hot-Stage AFM for Studying Thermo-mechanical Deformation in Microelectronic Devices

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Abstract

A commercial AFM was equipped with a hot-stage for conducting thermal cycling experiments up to 398K, as well as a vacuum and purge system to provide a protective environment during heating. Two different hot-stage configurations, one for studying features in the plane of a microelectronic device, and the other for studying features on its cross-section, were developed. It is shown that the AFM retains its calibration with no significant introduction of errors at temperatures up to 398K. Two applications of *in situ* hot-stage atomic force microscopy, related to microelectronic devices, have been demonstrated. First, the in-plane coefficient of thermal expansion of a low dielectric constant (low-k) thin film dielectric material used in back-end interconnect structures was measured. Secondly, the equipment was used to conduct *in-situ* studies of deformation of Cu thin film interconnect lines at the back end of silicon chips, under thermo-mechanical loads simulating those imposed on chip-level interconnect structures by a microelectronic package. The design of a bimetallic thermo-mechanical loading stage, which was used for the latter experiments in conjunction with the hot stage, is also discussed.

Key words: AFM, hot-stage, protective environment, thermo-mechanical loading

1. Introduction

Atomic force microscopy (AFM) is a widely used technique for surface characterization with nanometer scale resolution [1, 2, 3]. The rapid development of AFM instrumentation in recent years has significantly improved its capabilities, spurring considerable effort to develop AFM measurement approaches in a controlled temperature and environment in order to provide *in-situ* information on the sample under conditions of thermal excursions [4-11]. Although nominal temperature control in the AFM may be achieved by using a microheater and suitable control system in conjunction with the specimen stage, hot-stage AFM images are usually subject to significant thermal drift and distortions. A low-drift specimen stage design has been recently proposed to compensate for both in-plane (X-Y) and out-of-plane (Z) thermal drift [11]. Furthermore, in most modern AFMs, the scanning head has sufficient displacement range in all three directions to enable compensation of thermal expansion-induced movement of the specimen due to heating / cooling. The primary remaining challenge in the design of a hot-stage for an AFM, therefore, is due to the temperature-dependence of the piezoelectric constant of the piezo actuator (PZT stack) associated with the scanning device. This results in (a) alteration of the X-Y displacement calibration of the scanner, producing systematic, temperature-dependent errors in the measured dimensions of sample features, even when the temperature of the scan-head is nominally constant, and (b) image distortions due to small thermal transients which inevitably occur during a given scan, particularly when the sampling rate is low. The key problem to be addressed, therefore, devolves down to thermally isolating the PZT in order to keep its temperature as close to the ambient as possible, and to minimize its thermal fluctuations due to power variations of the sample heater controller.

For many applications, it is also desirable to conduct AFM studies in a controlled environment, such as vacuum, purge gas or a liquid. As a result, considerable recent effort has also focused on the design of environmental control of AFMs, e.g., for imaging in fluid [10], and vacuum [12]. To date, few studies have reported on the combination of thermal and environmental control of an AFM, particularly for non-biological samples.

Currently, there is significant interest in studying thermo-mechanical deformation of features within microelectronic devices and packages, which results from thermal expansion mismatch between the various disparate components of a package. In a typical microelectronic package, a silicon device, which contains numerous deep sub-micron to nano-scale metallic interconnect lines embedded in a thin film dielectric, is attached to an organic substrate via tiny, ball shaped solder joints. During thermal excursions associated with normal service, the thermal expansion mismatch between the organic substrate and the silicon chip produces substantial strains in the solder joints, as well as the composite back-end layer constituted by the interconnect lines embedded in dielectric, posing serious reliability problems. As feature-scales in microelectronic devices and packages continue to shrink due to increasing levels of integration, and as new materials are implemented in devices, the chip is being subjected to progressively larger package-level thermo-mechanical loads. As a result, there has emerged an acute need for novel metrology techniques, which enable studies of deformation fields in electronic devices under thermo-mechanical loads. Because of its high spatial resolution, the AFM offers an attractive tool to study the thermal deformation of device features [13,14], particularly as the critical dimensions of these features approach nanometer scales.

In this paper, we report on equipping a commercial AFM (VISTA-100 from Burleigh Instruments) with a hot-stage for thermal cycling up to 398K, and a vacuum and purge system to provide a protective environment during heating. In order to demonstrate its capabilities, we also report on the use of this equipment to conduct in-situ measurements of the coefficient of thermal expansion of low dielectric constant (low-k) dielectric lines on silicon microelectronic devices, as well as studies of deformation of Cu/low-k dielectric structures at the back end of silicon chips.

2. Design of Instrumentation

2.1 Controlled-atmosphere chamber

Since thin metallic films may be readily oxidized [15], and because acoustic isolation and the elimination of air currents is crucial for attaining optimum resolution in the AFM [16,17], the construction of a controlled-atmosphere chamber is critical to the

accuracy of any variable-temperature AFM study. Therefore, a controlled-atmosphere enclosure was built for the AFM. The chamber, which is shown in Figure 1, was attached to a mechanical vacuum pump as well as a source of a slightly reducing forming gas (98% Argon, 2%H_2), and was capable of an ultimate pressure of ~2 x 10^{-2} torr. This arrangement allowed successive evacuation and forming gas purge cycles to be implemented in order to lower the oxygen content below 10ppm, thereby limiting the oxidation of the sample to negligible levels during experimentation.

The basic construction of the environmental chamber began with a Pyrex bell jar of 0.457m diameter and 0.457m height, which was placed on a polished stainless steel baseplate. A Viton gasket was used to seal the surface between the bell jar and baseplate. The entire AFM was inserted into the bell-jar chamber, after replacing all plastic cables and attachments that were subject to out-gassing with vacuum-suitable alternatives. All connecting wires between the AFM and the computer, as well as heater wires and thermocouple cables, were passed through stainless steel tubing welded to the bottom of the bell-jar chamber, and emerged through standard vacuum feed-throughs for service connections. The entire set-up was mounted on a gas-charged vibration isolation table in order to de-sensitize the apparatus form disturbances from the ambient.

2.2 Controlled-temperature hot-stage

The ability to thermally load specimens *in-situ* while simultaneously imaging a material extends the potential of any microscopy. However, in an AFM, the construction of a hot-stage poses a number of challenges. Temperature and electrical transients need to be adequately controlled so that their effects on the various components of the AFM, such as the PZT, sensor tip, condenser mirrors and laser do not affect imaging accuracy and control. In addition, many components of the scanning module may suffer physical damage at elevated temperatures (e.g., soldered connections within the scan module), requiring the design of the hot-stage to focus primarily on safely elevating sample temperature while retaining signal fidelity.

Two different hot-stage designs were developed for different sample orientations. The first stage (horizontal hot-stage) was designed for studying features on the surface of

a microelectronic device, where the device-plane is parallel to the stage. The second stage (vertical hot-stage) was designed to study features on the cross-section of the device, where the device is placed on the stage edge-on.

The basic designs of the hot-stages are shown in Figure 2a, 2b and 2c. The horizontal hot-stage, shown in Figure 2a and 2b, uses a commercial channel strip heater (watt density ~ 4W/cm^2), which was mounted in a glass-ceramic housing, which in turn was attached to the sample stage of the AFM. The low thermal conductivity (K~0.6W/m-K) ceramic housing minimized conductive losses from the heater to the metallic body of the AFM, thereby limiting the power requirements and cycling times required of the heater controller to maintain a constant sample temperature. In order to minimize hot spots on the sample, a 0.005m thick Cu plate, which served as a heat redistribution layer, was attached to the top of the heater with a thermally conductive adhesive tape. In order to reduce instabilities due to stray electric fields between the tip and the heater, a grounding wire was solder-connected to the copper plate. The sample was then affixed to the copper plate through the use of thermally conductive adhesive tape. A fuzzy logic driven proportional-integral-differential (PID) controller was used in conjunction with a K-type thermocouple to control the sample temperature. The chromel and alumel wires of the control thermocouple were spot-welded directly to the copper plate on either side of the sample as shown in Figure 2b. This arrangement produced a low-profile thermocouple attachment, and was found to yield better temperature control at the sample than having the thermocouple on one side of the specimen. A separate thermocouple was also used to monitor the nominal stage temperature, which was maintained to within ±0.1K during all experiments.

The vertical hot-stage, which is shown in Figure 2c, uses two identical miniature resistive film heaters (watt density ~ 3 W/cm^2), one on either side of the specimen, which are vertically mounted on two ceramic blocks comprising parts of a ceramic housing. A grounded copper plate was attached to each heater, and temperature control was achieved through a flat-profile precision foil thermocouple affixed to one of the copper plates. As before, a separate thermocouple was used to independently monitor the sample temperature. The entire arrangement, including the ceramic housing, was attached to a

high-resolution X-Y translation stage with a displacement accuracy of ±1μm, which was then mounted on the standard micrometer stage of the AFM. The high-resolution stage afforded the coarse control necessary for placing the sub-micron features of interest close to the AFM tip, the final placement being accomplished by electronically moving the tip.

For both the horizontal and vertical configurations, two layers of insulating Kapton sheets (total thickness ~ 0.5μm) were placed around the specimen after mounting it on the hot-stage, as shown in Figures 2a and 2c. This arrangement completely covered the surface of the hot-stage, keeping only the specimen exposed, thereby minimizing convective and radioactive heating of the scan-head from the hot-stage. In addition to being thermally insulated from the hot-stage as best as feasible, the AFM head was actively cooled via an aluminum plate attached to one side, as shown in Figure 1. The Al plate was attached to a copper rod, which emerged from the environmental chamber through one of the feedthroughs, and had a braided end, which was immersed into a dewar-flask containing a mixture of methanol and liquid nitrogen at 233±10K. A fine-gauge thermocouple wire was attached to the probe-mounting fixture in the scan-head to estimate the probe and PZT stack temperature during the scan. Using the thermal management system described above, the tip/stack temperature could be maintained to within ±1K of the ambient temperature.

3. Experimental results and discussion

3.1 Validation of hot-stage AFM

Following addition of the hot-stage, the calibration of the AFM was checked using a standard silicon sample containing 1μm-wide surface grooves having a nominal pitch of 2.5μm and depth of 100nm, with a step-height accuracy of 1.5nm. Although not specifically fabricated for lateral calibration, the sample offered a grating that was very similar in design to typical metallic thin film interconnect line structures on electronic devices, making it a good calibration standard.

For the experiments, the environmental chamber was first evacuated to ~ 5 x 10^{-2} torr, using several fill-and-purge cycles as described before. The vacuum pump was then

switched off to minimize vibrations, and the chamber was backfilled with forming gas to a final pressure of ~1 torr. This prevented oxidation of the sample during cycling and enhanced thermal stability of the AFM.

Once a controlled atmosphere was established, experimental scans of the calibration grating were conducted *in situ* at 298K, 348K, and 398K. The sample was heated to the desired temperature at a nominal heating rate of 20K/min, with the AFM scan module in the raised position. Once the desired temperature was achieved, the scan module was lowered to the engaged position, and the system was thermally equilibrated till the variation of the specimen and scan-head temperatures were no more than 0.1K/hr. and 0.5K/hr., respectively. Typically, this was achieved in less than 15 minutes.

In order to achieve as high a lateral spatial resolution as feasible, scans were conducted in the contact-mode, using a force constant of 35nN and a scanning frequency of 2Hz. Figure 3 shows AFM images obtained from scans on the grooved silicon specimen at room temperature (Figure 3a), at 398K without environmental protection (Figure 3b), and at 398K with environmental protection (Figure 3c). In the absence of environmental control at 398K, even when the sample and tip reached nominal thermal equilibrium, proper alignment of the laser with respect to the split detector proved challenging due to thermal-expansion related drift of the mechanical fixtures of the laser-alignment mirrors as a result of minor temperature fluctuations. As shown in Figure 3b, these small temperature fluctuations ($< \pm 1$K) are reflected in a distorted AFM image, where the waviness of the image is due to time-dependency of the scan-head temperature during a scan. In order to circumvent this, the lower part of the metallic scan-head case was covered with a black thermally insulating plastic sheet (~0.5mm thick), and then wrapped with an Al foil, as indicated in Figure 1. The reflective side of the Al foil was directed outward, in order to minimize radiative heating of the scan head from the hot-stage. With this change and following implementation of environmental control, the AFM image was nearly distortion-free, as shown in Figure 3c. A small systematic error in the z-direction was noted, leading to the slight surface waviness observed in Figure 3c, but this could be largely compensated for via software control during post-processing.

From the images obtained above, the surface profiles of the sample along several lines perpendicular to the axis of the grooves were computed. Figure 4 shows the profiles of several alternating Si lines and grooves at roughly the same location, obtained at 298K and 398K. No evidence of distortion in the line profile for 398K is noted upon comparing it to that for 298K. These line profiles were used to compute the coefficient of thermal expansion (CTE) of the Si standard. Figure 5 shows the cross-sectional profile of one Si line. Since the width of the Si line near the bottom of the groove is convoluted with artifacts associated with the scanning rate and tip-geometry, the CTE was calculated using the width at the top surface of the Si lines, as shown in Figure 5. About 90 separate profiles obtained from the same line were measured, and the mean line width at a given temperature was determined from the distribution. The in-plane CTE of the LKD was then determined from the slope of the mean line width vs. temperature plot. The histograms of measured line width at each temperature, and the plot for determining CTE are shown in Figure 6. The means and standard deviations of the line widths and line thickness as determined from the AFM line-scans are summarized in Table1. The CTE of Si thus measured is 2.92×10^{-6}/K, which is very close to the reference value of 2.8×10^{-6}/K for [100] Si reported in the literature [18]. This clearly demonstrates that the AFM retains its x and y-calibration till 398K.

Whereas in the lateral direction, the line-width clearly increased with increasing temperature, no measurable change in the line thickness was noted at different temperatures. This is principally because, for the 100nm line thickness of Si, the increase in height over a temperature range of 100K is only 0.029nm (for $CTE_{Si} = 2.9 \times 10^{-6}$/K), whereas for the 100nm step height of the present sample, the minimum detectable change could be about 1nm (1% of 100nm). Although changes in the line thickness are not detectable, it is clear from Table 1 that the actual out-of-plane dimension of the Si line is measurable to within ±1nm up to 398K, suggesting that the AFM retains its z-calibration up to this temperature.

From the above, we may infer that the design of the hot-stage reliably reflects the critical dimensions of the specimen in both in-plane and out-of-plane directions over the range 298K through 398K. Importantly, it is noted that the width of the distributions in

Figure 6 does not change appreciably with temperature, suggesting that the measurement errors do not have any significant temperature dependence up to 398K.

3.2 Application of the Hot-stage AFM to Microelectronic Devices.

Atomic force microscopy has been previously utilized to characterize thermo-mechanical deformation and interfacial sliding in thin film on substrate [19-21] and back-end interconnect structures (BEIS) of microelectronic devices [16,17,22]. Here we present results on two separate uses of *in situ* hot-stage atomic force microscopy: (1) to measure the CTE of low dielectric constant (low-k) thin films which are used in back-end structures of microelectronic devices, and (2) to study the distortion of Cu interconnect lines embedded in a low-k dielectric (LKD) under loading conditions similar to those imposed on a device by the microelectronic package.

3.2.1 Determination of CTE of Low-k Dielectric Film

The sample used for the first set of experiments consisted of one layer of 350nm thick, alternating parallel Cu and LKD lines on Si, as shown in Figure 7. The width of the Cu lines, which were surrounded on the sides and bottom by a 35nm thick Ta barrier layer, varied from 0.2 to 1.8μm, with the corresponding LKD width ranging from 1.4 to 1.1μm. This sample, fabricated via the damascene process using a hybrid organic/inorganic silicate-based LKD with a k value of approximate 2.5, was chemo-mechanically polished (CMP) to produce a nominally flat surface. The Cu lines were then etched off completely by immersion in a solution of 3 gm/liter of sodium persulfate ($Na_2S_2O_8$) in 2% H_2SO_4, leaving the LKD lines unaffected. Although the etching did not remove the 35nm Ta barrier layer, this layer provides negligible lateral constraint on the much wider (1-1.4μm) LKD lines, and therefore is not expected to influence to measured CTE data. Figure 8 shows an AFM image of the surface of the sample following etching of the Cu. The in-plane CTE of the low-k dielectric material was then measured using the same procedure as that used on the Si calibration sample. Although the dimensions of the LKD line near the bottom (i.e., the line-substrate interface) are affected by thermally induced in-plane (IP) stresses (σ_{LKD}^{IP}) due to CTE mismatch between LKD and Si, by conducting the measurements at the top surface of the line, where $\sigma_{LKD}^{IP} \approx 0$,

complications due to residual stresses were avoided. As for the Si calibration sample, at least 50 separate profiles obtained from the same line were measured, and the mean line width at a given temperature was plotted against temperature to yield the in-plane CTE. In principle, the out-of-plane CTE is also determinable from the same experiments. However, for the 350nm thickness of the present LKD lines, the OOP expansion of the line due to a 100K temperature change would only be ~0.175 to 0.7 nm for a CTE range of $5x10^{-6}$/K to $20x10^{-6}$/K. Since the OOP resolution of most AFMs is limited to about 1% of the total OOP displacement range, in this case, no less than a 3.5nm OOP displacement would be measurable with confidence. Therefore, only the CTE in the IP direction was measured in the present work.

Figures 9a-c shows histograms of the LKD line-width distribution at 293K, 348K and 398K. The widths display a nominally Gaussian distribution at all three temperatures. Quite clearly, the mean of the distribution increases with increasing temperature, the variation of the mean line width with temperature being shown in Figure 9d. From the slope of the plot in Figure 9d, the in-plane CTE of the low-K dielectric was determined to be $4.9x10^{-6}$/K. Thus, the hot-stage AFM provides a capable tool for determining thermal expansion behavior of thin films of complex geometries deposited on various substrates.

3.2.2 Deformation of Interconnect Structures in Microelectronic Devices

A second type of sample, comprising a single layer of 350nm thick alternating Cu/LKD lines, capped by a 2000nm LKD layer, was used for studying deformation of Cu interconnect lines under far-field thermo-mechanical loads similar to those applied on a device by a flip-chip microelectronic package. The sample cross-section was revealed by micro-cleaving normal to the interconnect lines, followed by focused ion beam (FIB) polishing. An AFM image of the sample cross-section, showing alternating 0.5μm and 1.8μm-wide Cu lines embedded in LKD on Si, is shown in Figure 10a. The sample was mounted in a bi-metallic fixture constructed of Invar and Al, as shown in Figure 10b. The LKD side of the sample was bonded to the Al plate (CTE=$22x10^{-6}$/K) using a glass-filled epoxy (E=11GPa, CTE=$21x10^{-6}$/K), whereas the Si side was bonded to the Invar plate (CTE=$0.5x10^{-6}$/K) using a ceramic glue. During thermal cycling, this arrangement

allowed the BEIS to be placed in severe shear due to the CTE mismatch between Al and Invar. At any temperature T, the nominal maximum shear strain imposed on the chip is given by $\Delta\alpha\Delta T.x/t$, where $\Delta\alpha$ is the CTE difference between Al and Invar, ΔT is the difference between T and the ambient temperature, x (10mm) is the effective length of the bi-metallic fixture and t (~793μm) is nominally the sum of the thicknesses of the chip (t_{chip}=753μm) and the glue layers ($t_{ceramic\ glue}$ + $t_{underfill}$ ~40μm). In actuality, since the ceramic glue and Si are relatively stiff, the majority of the imposed shear deformation is likely to be concentrated in the compliant low-K layer and epoxy (which have low Young's moduli of 5-7 GPa and 11GPa, respectively). This allows the local shear strain within the Cu/low-K BEIS to be very large. For ΔT=100K, the shear strain in the BEIS may be estimated to be on the order of $\Delta\alpha\Delta T\ x/(t_{BEIS} + t_{underfill})$, which is ~0.5-1.

This set-up was mounted in the vertical AFM hot-stage and *in-situ* thermal cycling experiments (293-398K) were conducted. These experiments provide an effective means of simulating BEIS deformation due to CTE mismatch between a Si chip and the organic substrate to which it is attached in a flip-chip package, wherein a temperature-dependent shear strain is imposed on the BEIS as the package undergoes thermal cycling during service [22].

Figures 11a and 11b show the appearance of the sample cross-sections at 298K and 398K, respectively, showing the cross-sections of 3 Cu lines protruding out slightly from the planarized Si/LKD surface. Since the expansion of the bimetallic frame causes significant lateral movement of the sample during *in-situ* heating (~10-20μm for a 100K temperature change), the scans were conducted over a large area (20μm x 20μm) in order to avoid losing the area of interest during heating. Although the hot-stage is equipped with a precision translation-stage, the controls for the stage were located inside the bell-jar. Therefore, after heating to the relevant temperature, the bell-jar was briefly removed, the sample was moved by a predetermined amount, and environmental contol was re-established, before obtaining the elevated-temperature scans. This procedure invariably caused some movement of the sample, necessitating scanning over a large area in order to locate the feature of interest. Because of the requirement of a large scan area, the zoomed-in image appears pixellated, revealing the individual scan lines, and making the

images appear noisy, as seen in Figures 11a and 11b. This problem can be largely circumvented by using a remotely controlled stage, which would enable locating the feature of interest without breaking environmental control, and therefore eliminate the need for scanning large areas.

Despite the reduced lateral resolution of the present scans, the cross-section of a 0.5μm Cu line was tracked at different temperatures during *in-situ* cycling, and the locus of points along the perimeter of the line at an elevation of 20nm from the adjacent regions (Si or LKD) were recorded. This is shown in Figure 12. It is seen that the line undergoes significant shear distortion during heating to 398K, much of which remains upon cooling to 298K. This implies that the line is plastically deformed during thermal cycling. After 25 cycles, a net shear strain of ~0.15 is observed to have accrued in the Cu line. This type of 'film crawling', whereby a thin film line undergoes progressively increasing shear deformation with increasing number of cycles, is known to be a potential failure mechanism in metal/low-k dielectric interconnect structures [22,23]. Clearly, using the in-situ hot-stage AFM reported here, these deformation effects may be effectively studied. Furthermore, the approach may also be utilized to map the strain-fields within BEIS during thermo-mechanical cycling of packages, when used in conjunction with digital image correlation, which can then provide a fundamental understanding of the operative deformation mechanisms, in addition to providing experimental verification tools for modeling efforts.

4. Conclusions

A commercial AFM was equipped with a hot-stage for thermal cycling experiments up to 398K, as well as a vacuum and purge system to provide a protective environment during heating. Two different hot-stage configurations, one for studying features in the plane of a microelectronic device, and the other for studying features on its cross-section, were developed. Using a grooved silicon specimen, it is shown that the AFM maintains good lateral and z-calibration with no significant introduction of errors at temperatures up to 398K. This allows the AFM to be used for a variety of applications related to microelectronic devices. Two applications of *in situ* hot-stage atomic force

microscopy have been demonstrated, using the apparatus developed here. First, the in-plane coefficient of thermal expansion of low dielectric constant thin film lines used in interconnect structures in microelectronic devices was measured over the temperature range 298K-398K. Secondly, we report on the use of this equipment to conduct *in-situ* studies of deformation of Cu thin film interconnect lines at the back end of silicon chips, using a bi-metallic loading frame in conjunction with the hot-stage. These studies simulated conditions of thermo-mechanical cycling to which back-end structures of microelectronic devices are subjected during service in association with a package, and showed that during cycling, the Cu lines are plastically strained in shear, the strain ratcheting up with increasing number of cycles. Although the equipment reported here was developed for studying microelectronic devices, it may be used to study a variety of materials at temperatures up to 398K, where environmental protection from the ambient is of concern.

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FIGURES

Figure 1: Schematic of the controlled-atmosphere chamber and attachments for the AFM.

Figure 2: Schematics of (a) the horizontal hot-stage, (b) the heater assembly for the horizontal stage, and (c) the vertical hot-stage.

Figure 3: In-situ surface AFM scans for Si calibration sample at (a) 298K, (b) 398K with no environmental control, and (c) at 398K with environmental control.

Figure 4: AFM line profiles of the calibration grating, obtained at 298K and 398K.

Figure 5: AFM line-scan of the profile of a line of the Si calibration standard at 298K, showing the parameters used for determining the CTE of Si.

Figure 6: Histograms of the width distribution of Si lines at different temperatures (a-c), and the variation of the mean line width with temperature (d). The slope of the mean line width vs. temperature plot represents the in-plane CTE of the Si.

Figure 7: (a) Schematic of the sample with a single layer of Cu/Low-k dielectric interconnect structure. The structure consists of one layer of 350nm thick, alternating parallel Cu and LKD lines of different widths on a Si substrate. (b) Surface AFM image of the Cu/LKD structure after CMP.

Figure 8: AFM image of the single-layer Cu/LKD sample, following etching of the Cu lines, showing only LKD lines on Si.

Figure 9: Histogram of the width distribution of low-K dielectric lines at different temperatures (a–c), and the variation of the mean line width with temperature (d) The slope of the mean line width vs. temperature plot represents the in-plane CTE of the LKD.

Figure10: (a) An AFM image of the micro-cleaved and FIB polished cross-section of sample C, showing alternating 0.5μm and 1.8μm wide Cu lines embedded in LKD on Si. (b) Schematic of the bi-metallic fixture constructed of Invar and Al, on which the sample was mounted for simulating shear deformation of the back-end structure due to package-level stresses during thermal cycling.

Figure 11: *In situ* AFM scans of the cross section of a chip at (a) 298K and (b) 398K, showing a narrow Cu line and parts of two wider Cu lines, surrounded by LKD on 3 sides, and by Si on the other. The lines protrude out of the chip

cross-section because of the different rates of ion-beam polishing of Cu and Si/LKD.

Figure 12: Perimeter of the cross-section of a 0.5μm wide Cu line embedded in LKD at different stages of thermo-mechanical cycling between 298K and 398K, with the sample mounted in the bi-metallic fixture. During cycling, a nominal shear strain of 0.5 to 1 was imposed on the back-end structure in order to simulate the effect of far-field package-level stresses.

TABLE 1

Measured dimensions of line-grating on the Si calibration sample at various temperatures

Temperature	In plane: Width (nm)	Out of Plane: Thickness (nm)
298K	1580.92±1.30	97.57±0.83
348K	1581.16±1.25	98.38±0.96
398K	1581.42±1.44	96.86±0.79

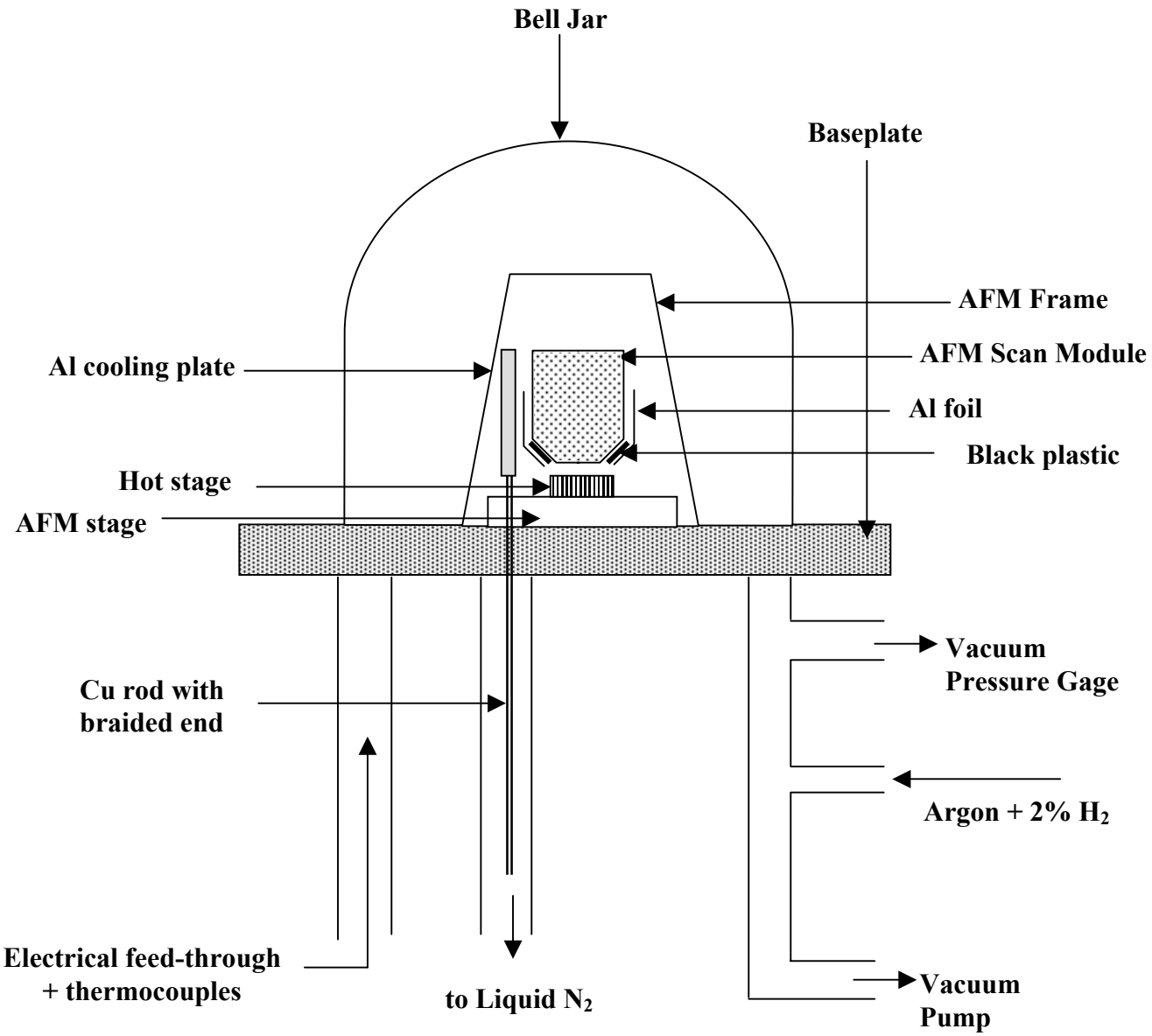
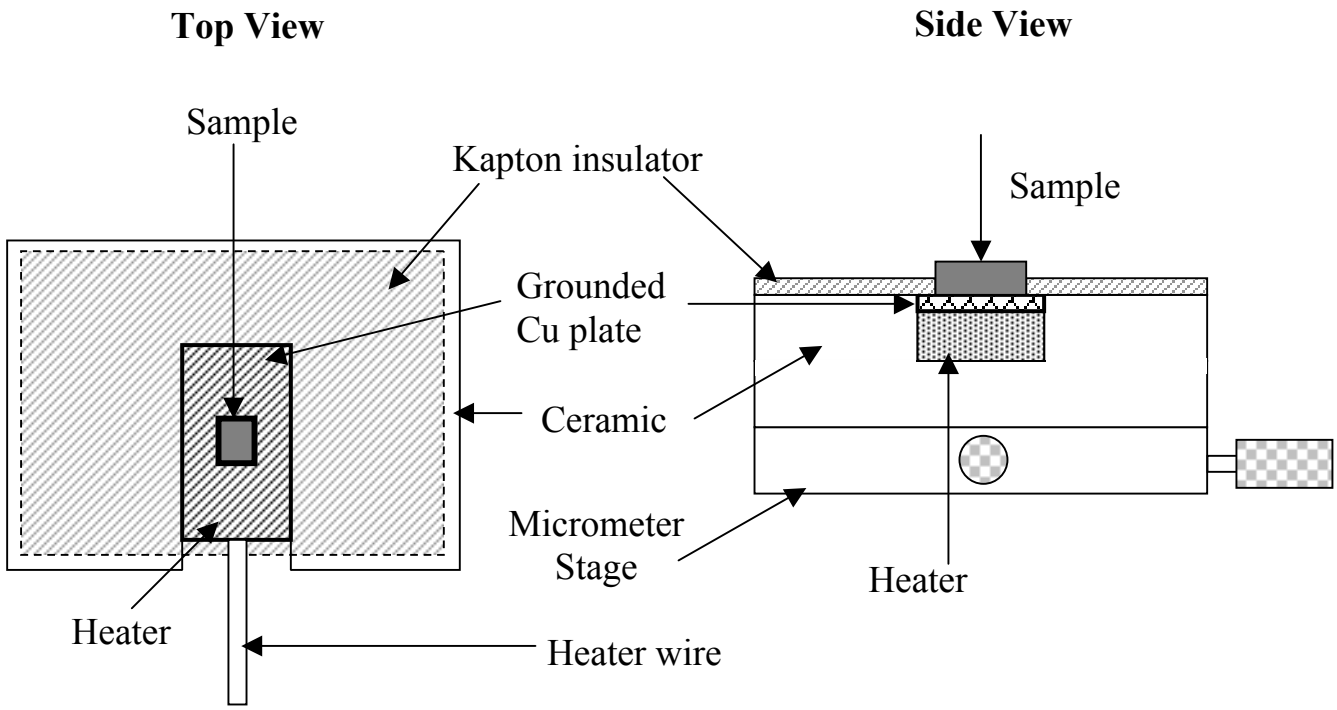
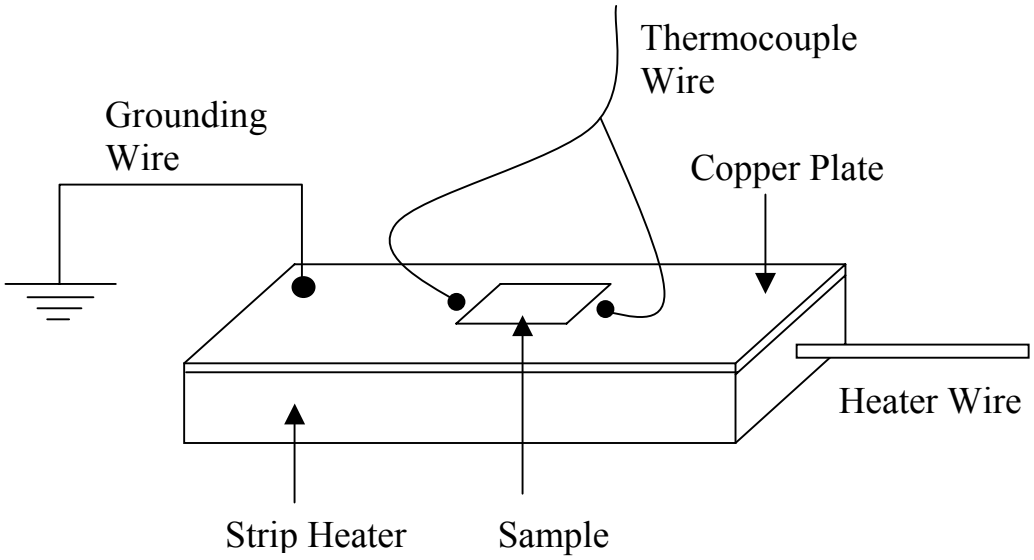


Figure1: Schematic of the controlled-atmosphere chamber and attachments for the AFM



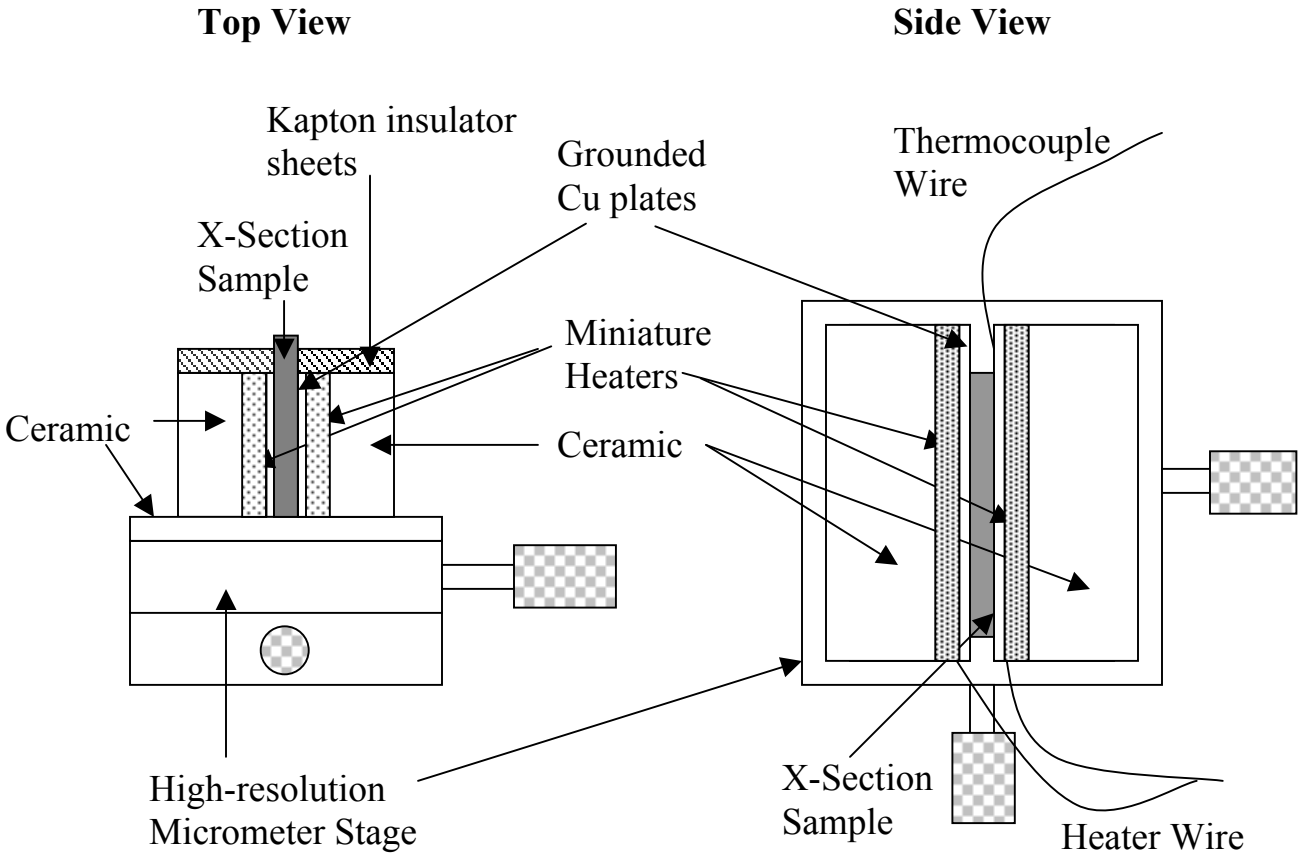
(a)



(b)

Figure 2: Schematics of (a) the horizontal hot-stage, (b) the heater assembly for the horizontal stage, and (c) the vertical hot-stage.

(figure contd. on next page)



(c)

Figure 2: Schematics of (a) the horizontal hot-stage, (b) the heater assembly for the horizontal stage, and (c) the vertical hot-stage.

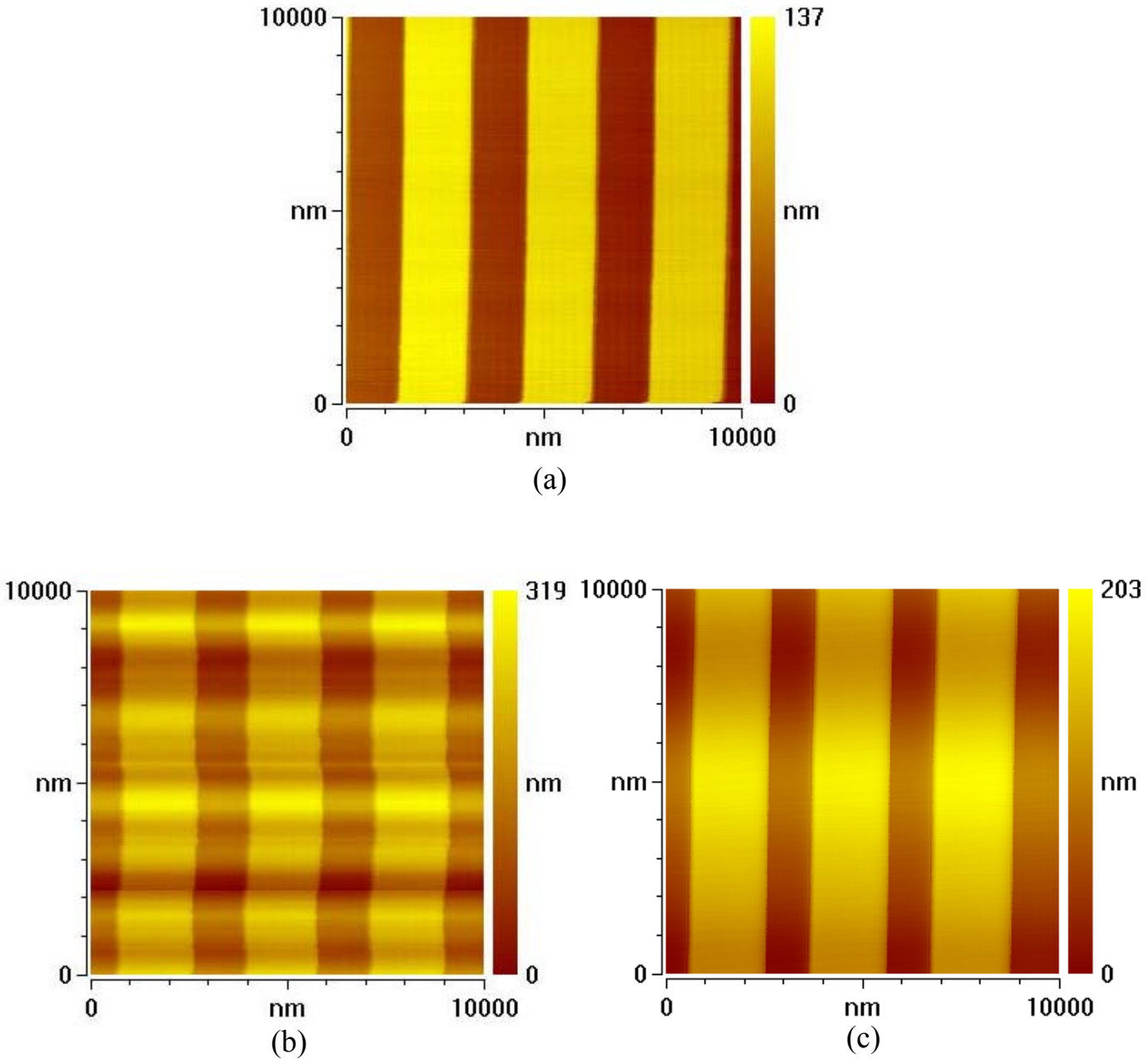


Figure 3: In-Situ surface AFM scans for Si calibration sample at 298K (b) 398K with no environmental control, and (c) at 398K with environmental control.

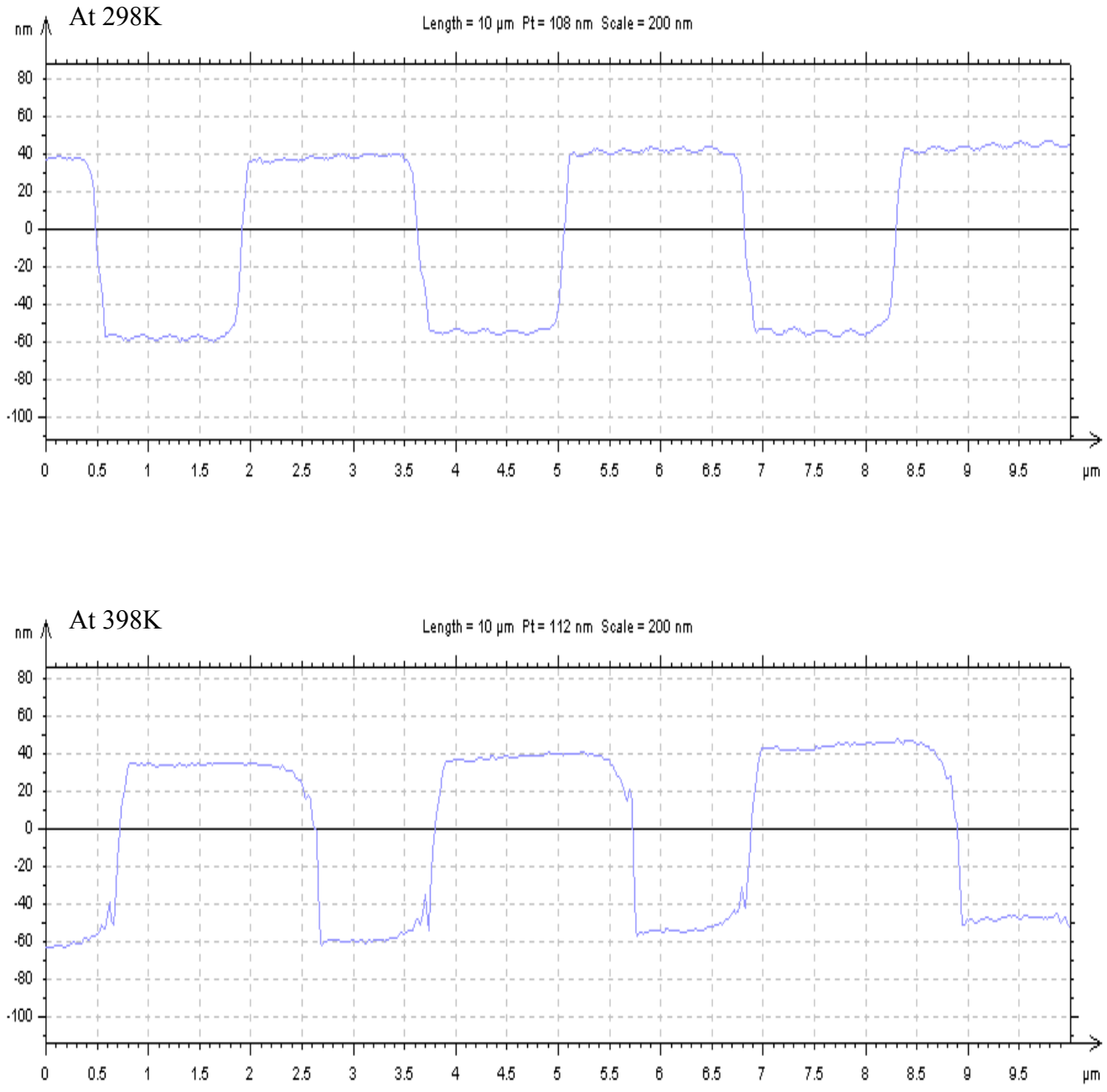


Figure 4: AFM line profiles of the calibration grating, obtained at 298K and 398K.

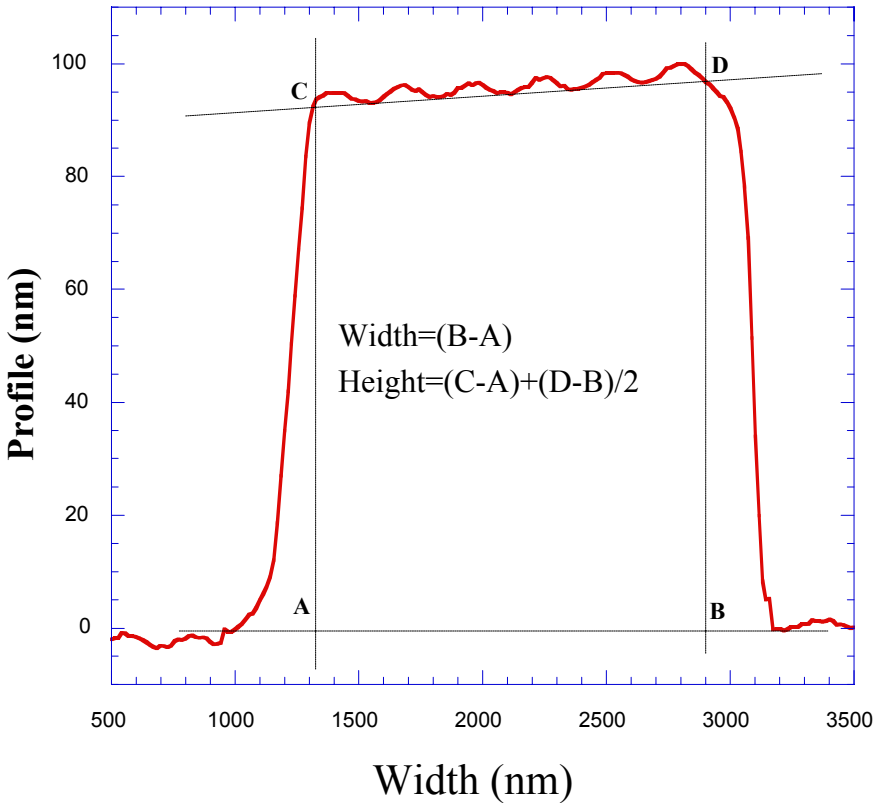


Figure 5: AFM line-scan of the profile of a line of the Si calibration standard at 298K, showing the parameters used for determining the CTE of Si.

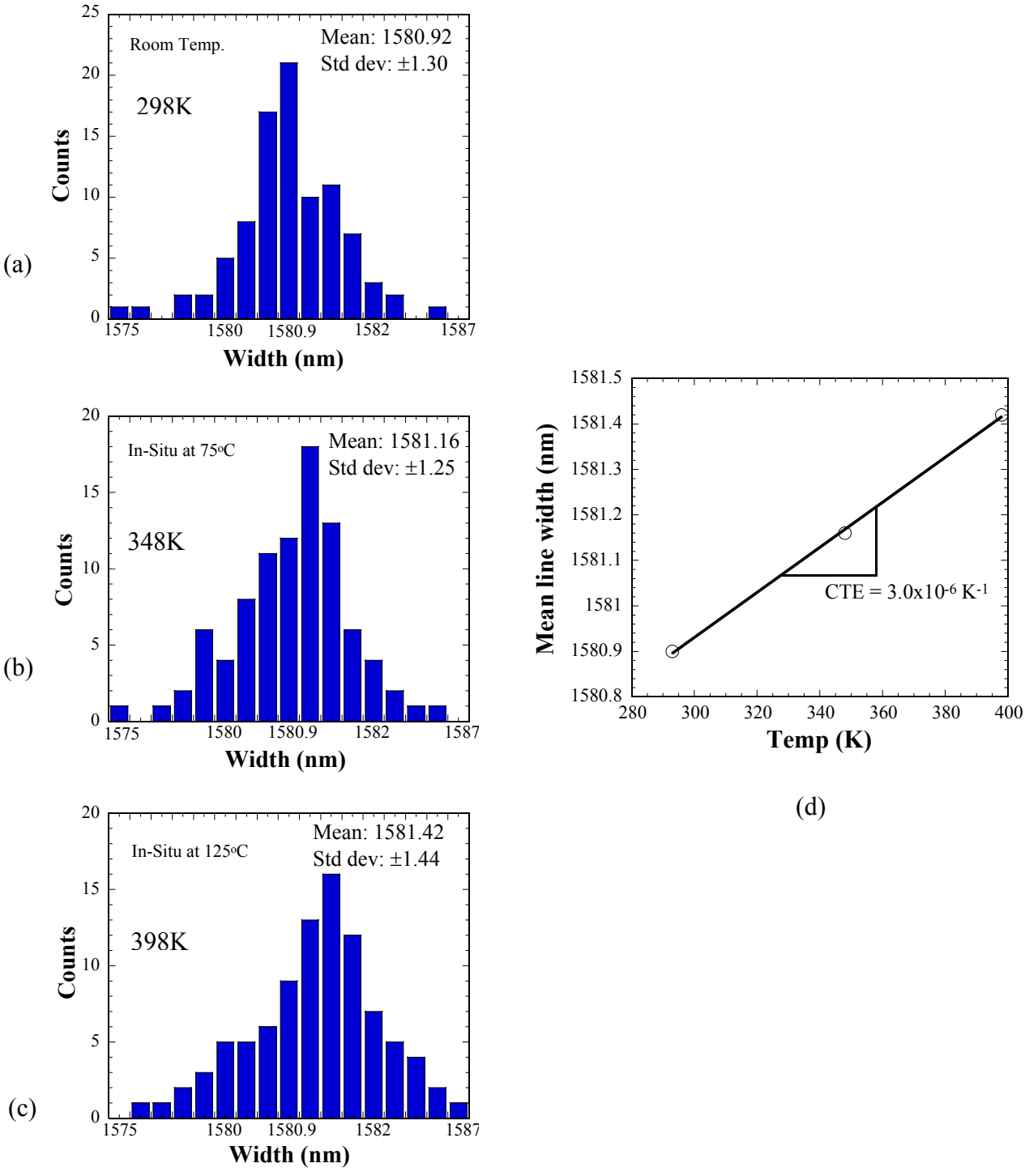
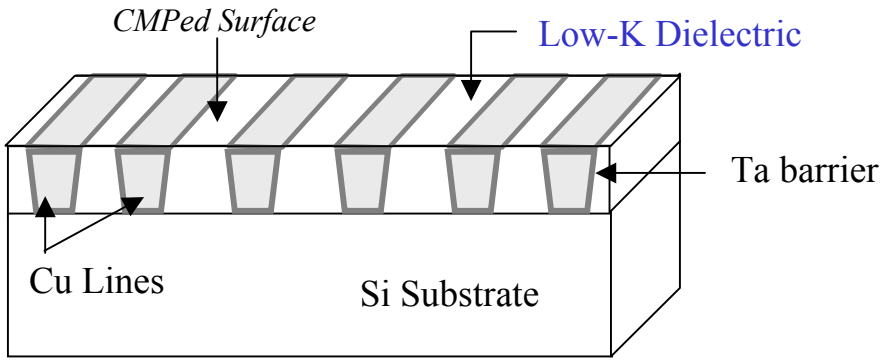
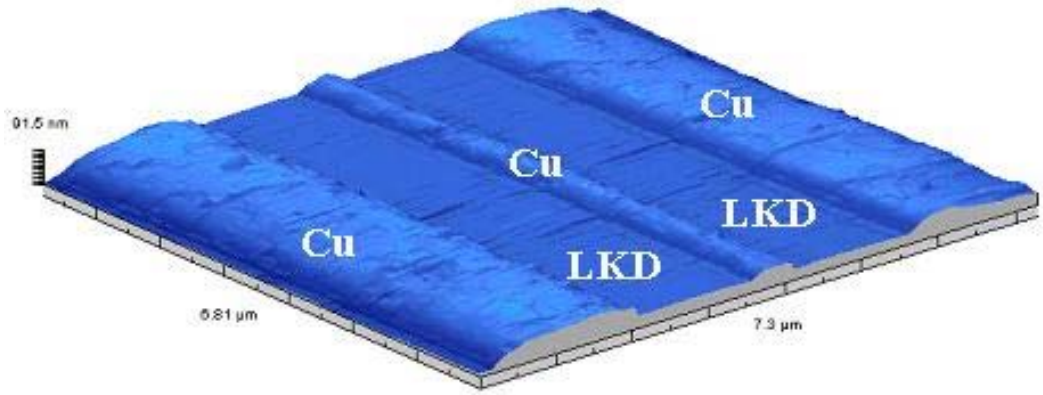


Fig. 6 Histograms of the width distribution of Si lines at different temperatures (a-c), and the variation of the mean line width with temperature (d). The slope of the mean line width vs. temperature plot represents the in-plane CTE of the Si.



(a)



(b)

Figure 7: Schematic of the sample with a single layer of Cu/Low-k dielectric interconnect structure. The structure consists of one layer of 350nm thick, alternating parallel Cu and LKD lines of different widths on a Si substrate. (b) Surface AFM image of the Cu/LKD structure after CMP.

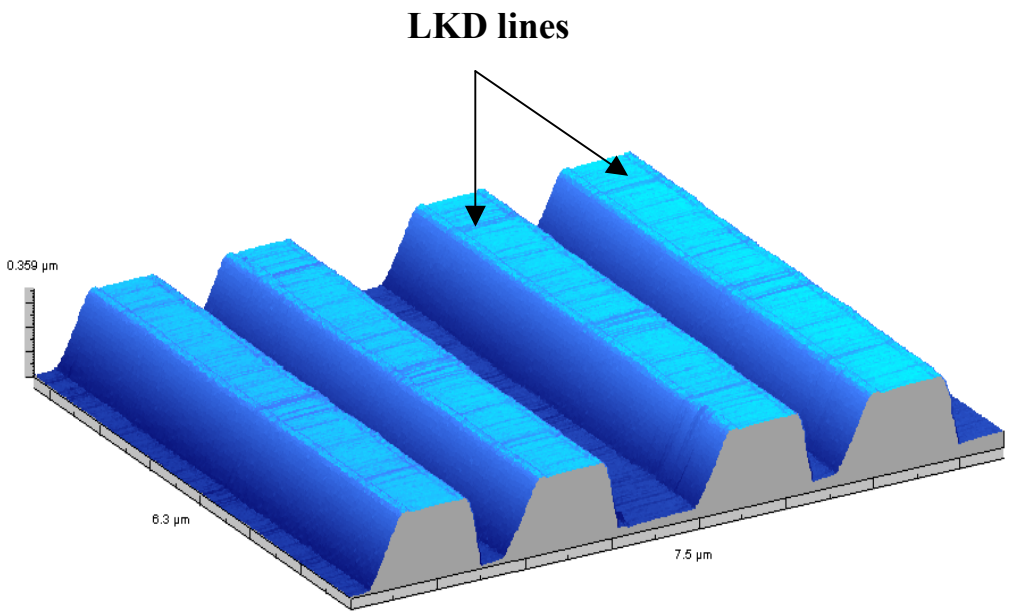


Figure 8: AFM image of the single-layer Cu/LKD sample, following etching of the Cu lines, showing only LKD lines on Si.

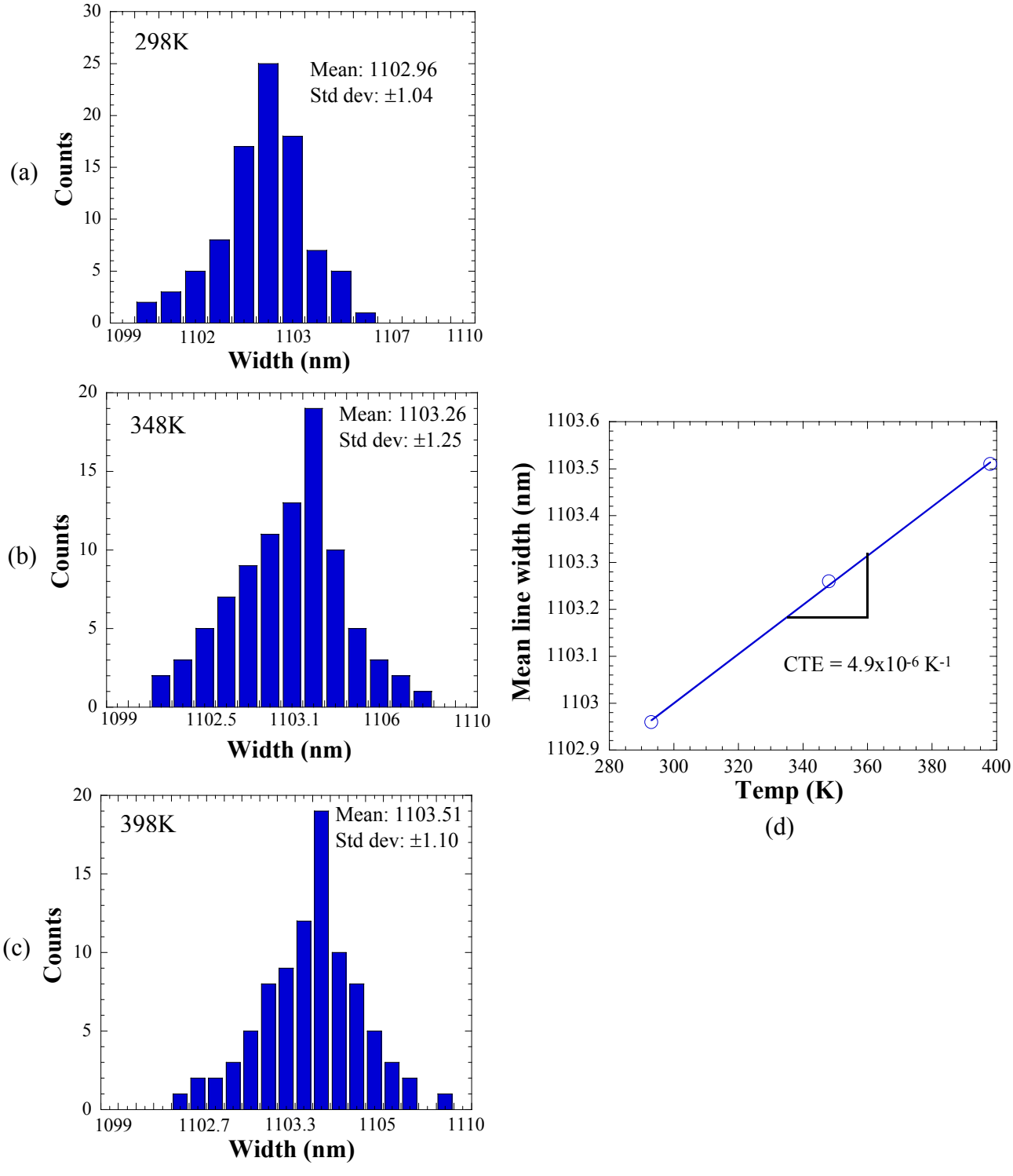
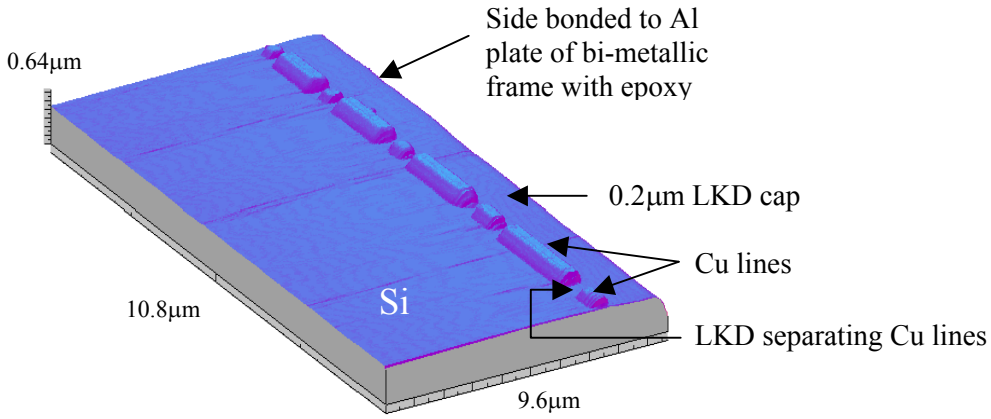
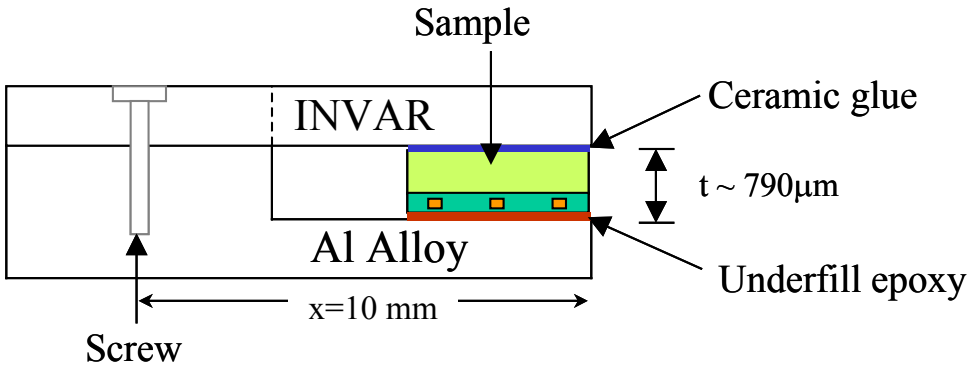


Figure 9: Histogram of the width distribution of low-K dielectric lines at different temperatures (a – c), and the variation of the mean line width with temperature (d) The slope of the mean line width vs. temperature plot represents the in-plane CTE of the LKD.

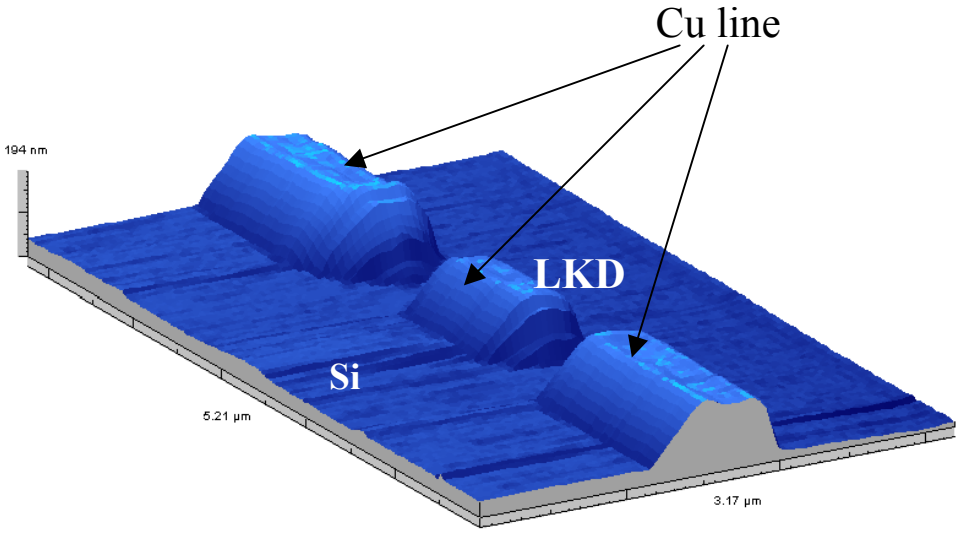


(a)

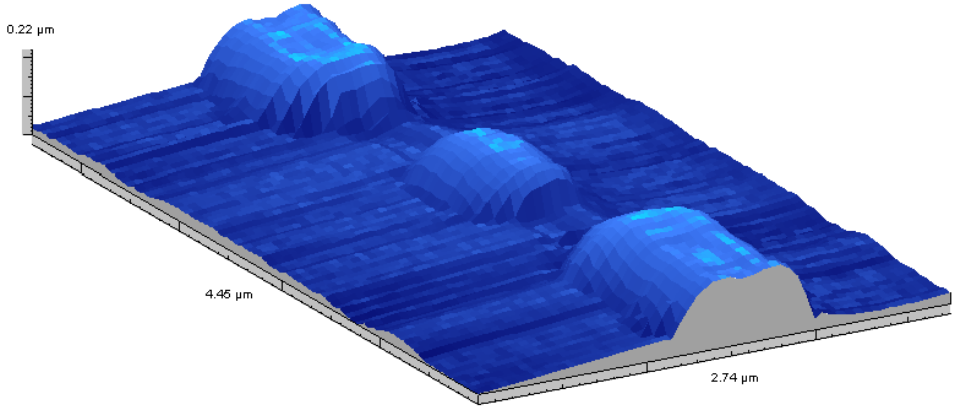


(b)

Figure 10: (a) An AFM image of the micro-cleaved and FIB polished cross-section of sample C, showing alternating 0.5µm and 1.8µm Cu lines embedded in LKD on Si. (b) Schematic of the bi-metallic fixture constructed of Invar and Al, on which sample C was mounted for simulating shear deformation of the back-end structure due to package-level stresses during thermal cycling.



(a)



(b)

Figure 11: *In situ* AFM scans of the cross section of a chip at (a) 298K and (b) 398K, showing a narrow Cu line and parts of two wider Cu lines, surrounded by LKD on 3 sides, and by Si on the other. The lines protrude out of the chip cross-section because of the different rates of ion-beam polishing of Cu and Si/LKD.

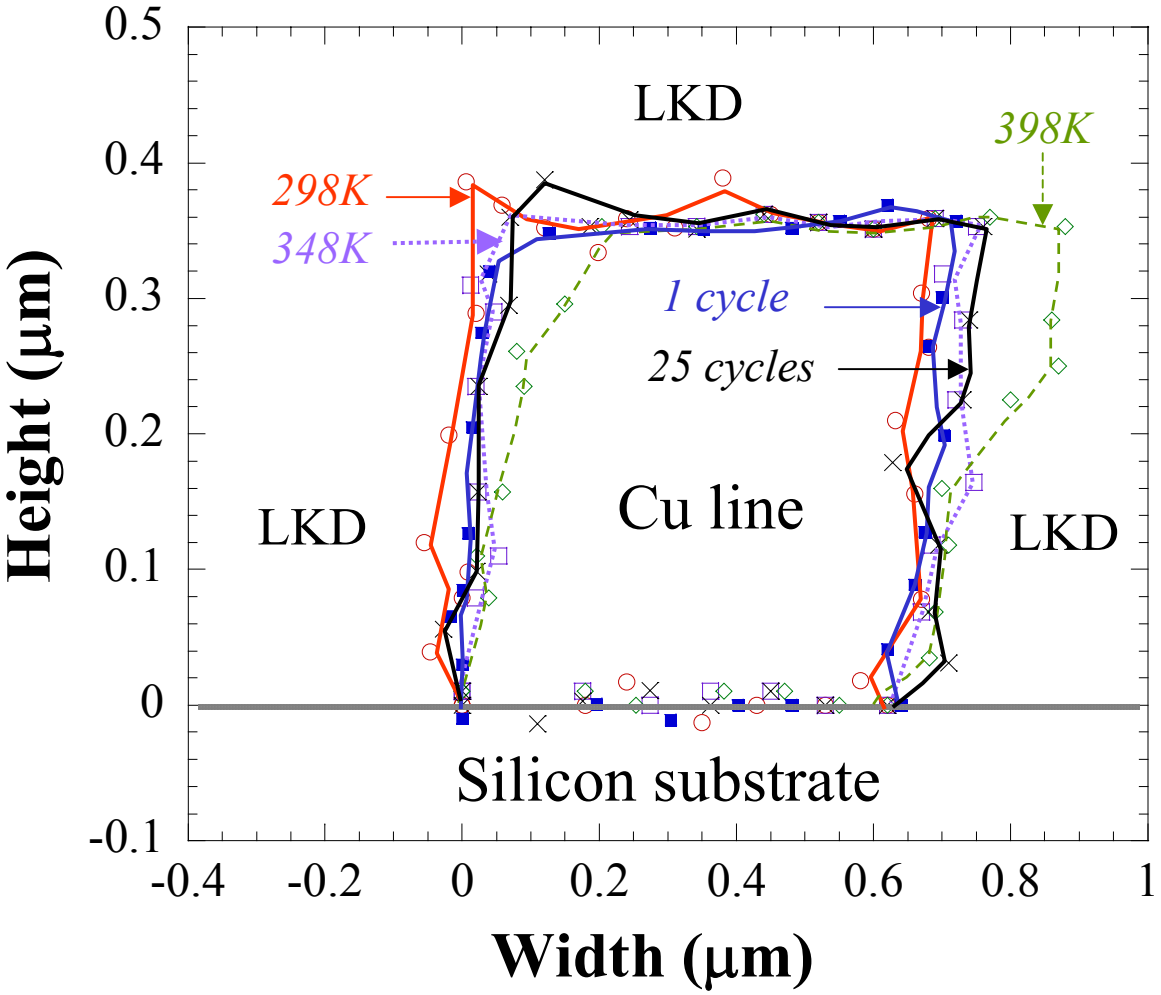


Figure 12: Perimeter of the cross-section of a 0.5μm wide Cu line embedded in LKD at different stages of thermo-mechanical cycling between 298K and 398K, with the sample mounted in the bi-metallic fixture. During cycling, a nominal shear strain of 0.5 to 1 was imposed on the back-end structure in order to simulate the effect of far-field package-level stresses.